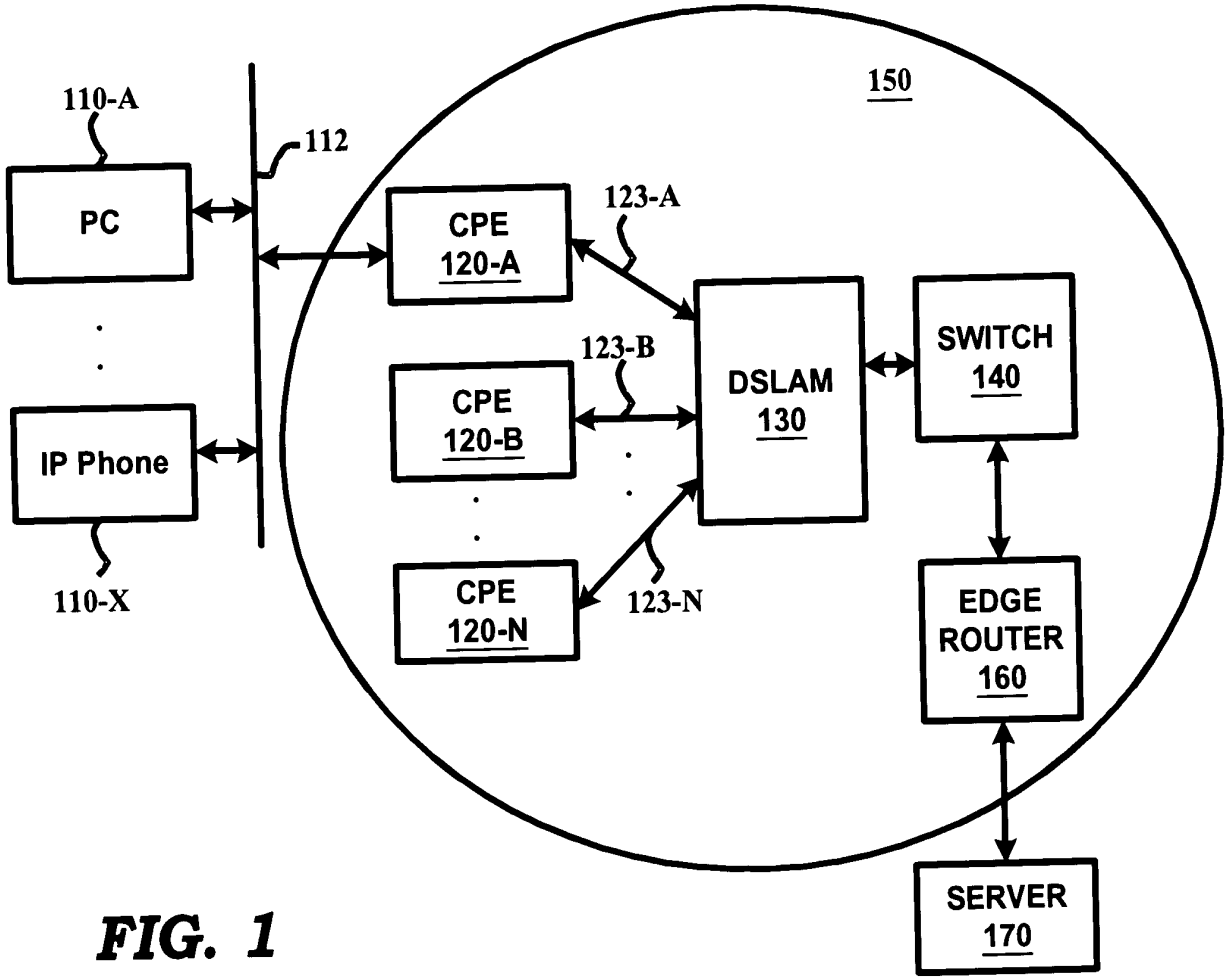

150
110-A
112
PC
CPE
120-A
123-A
123-B
CPE
120-B
DSLAM
130
SWITCH
140
IP Phone
110-X
CPE
120-N
123-N
EDGE
ROUTER
160
SERVER
170

FIG. 1

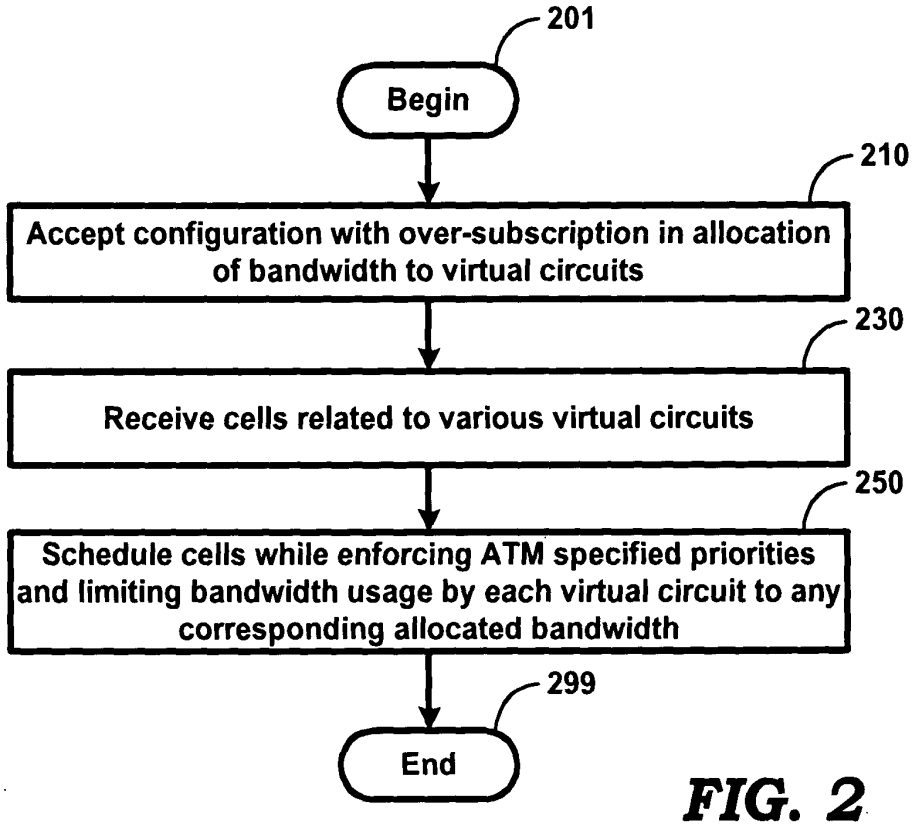

201
Begin
210
Accept configuration with over-subscription in allocation of bandwidth to virtual circuits
230
Receive cells related to various virtual circuits
250
Schedule cells while enforcing ATM specified priorities and limiting bandwidth usage by each virtual circuit to any corresponding allocated bandwidth
299
End

FIG. 2

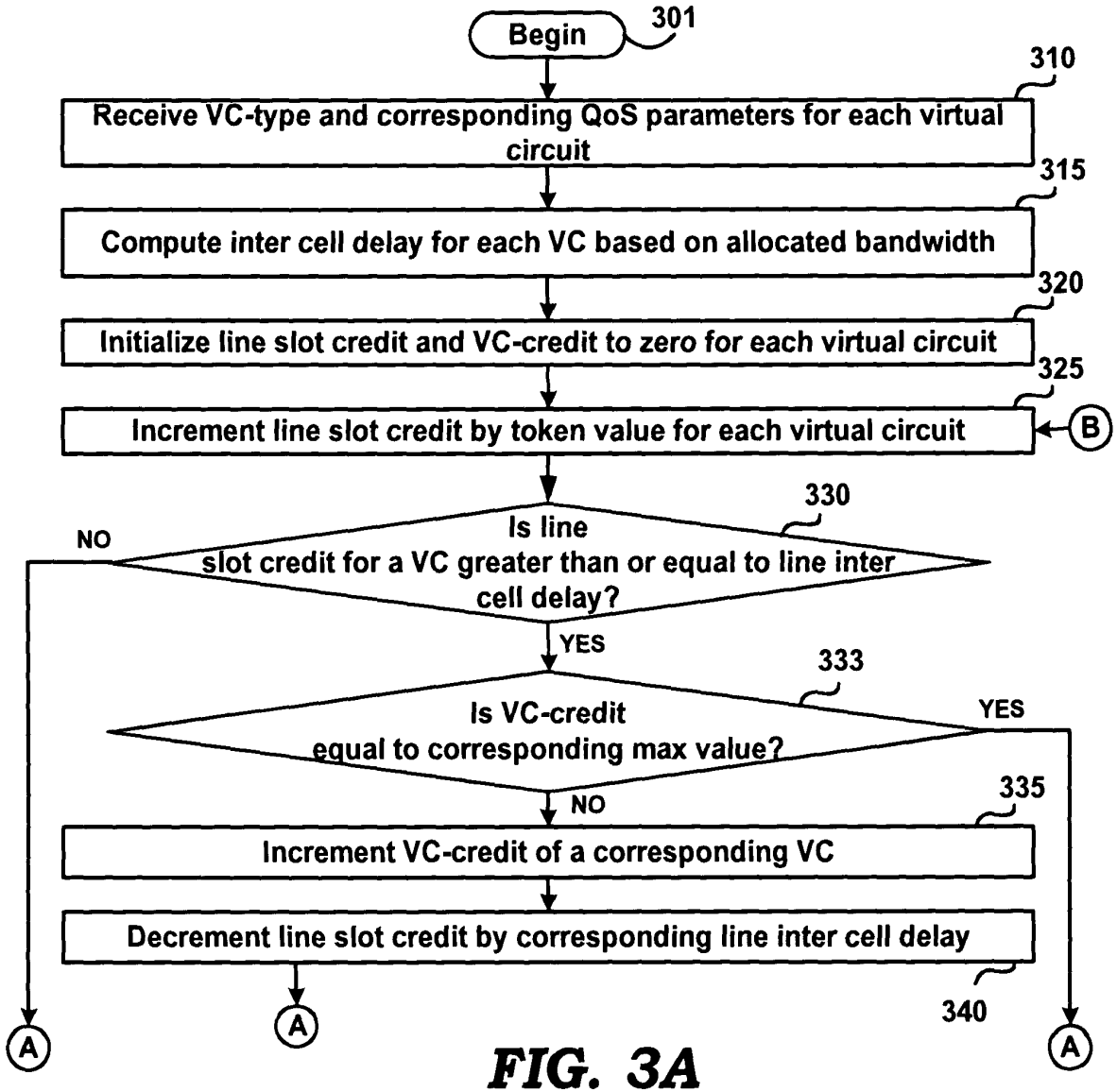
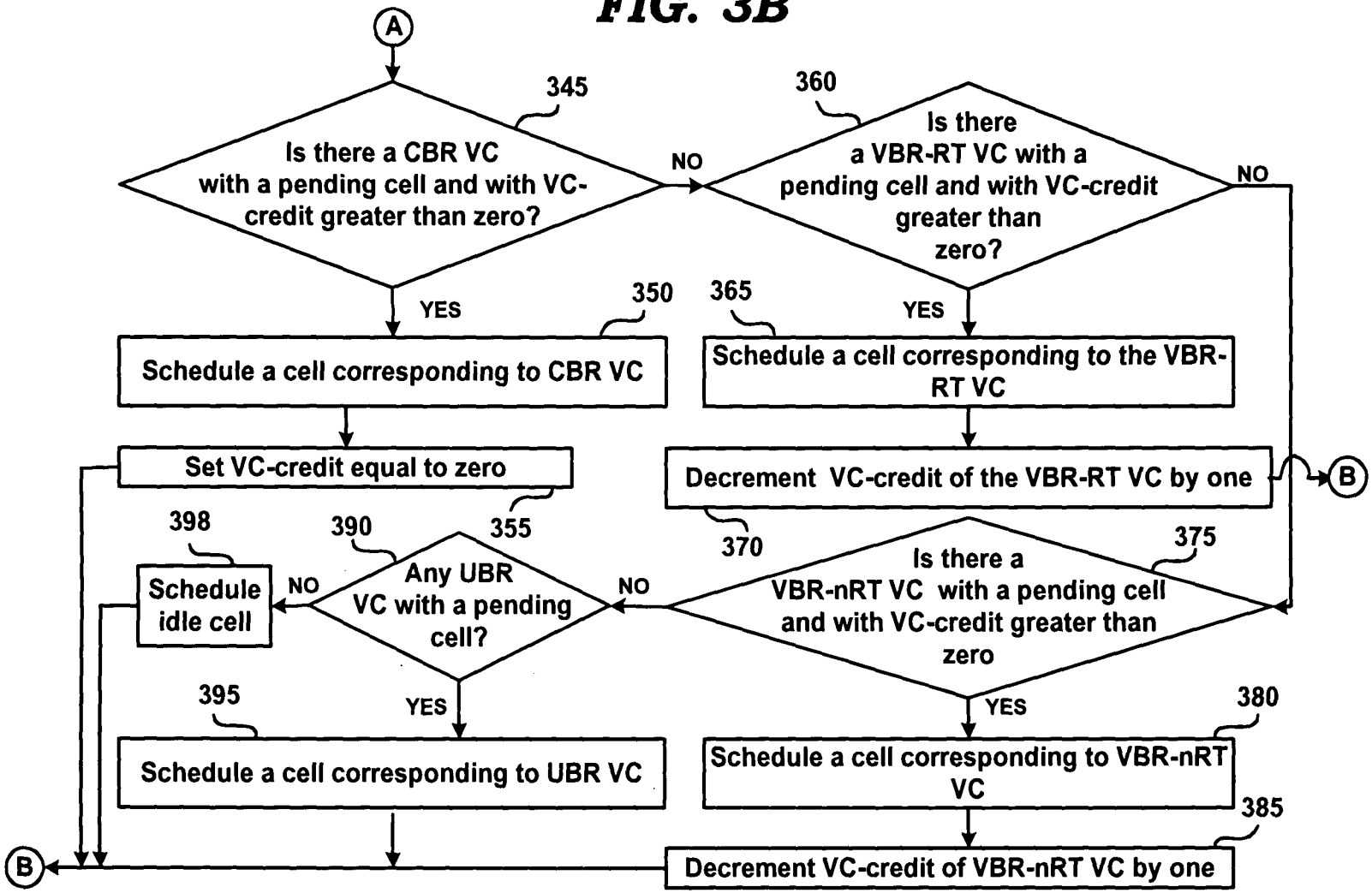

Begin
301
310
Receive VC-type and corresponding QoS parameters for each virtual circuit
315
Compute inter cell delay for each VC based on allocated bandwidth
320
Initialize line slot credit and VC-credit to zero for each virtual circuit
325
Increment line slot credit by token value for each virtual circuit
B
330
Is line slot credit for a VC greater than or equal to line inter cell delay?
NO
YES
333
Is VC-credit equal to corresponding max value?
YES
NO
335
Increment VC-credit of a corresponding VC
Decrement line slot credit by corresponding line inter cell delay
340
A
A
A

FIG. 3A

FIG. 3B


A
345
Is there a CBR VC with a pending cell and with VC-credit greater than zero?
NO
360
Is there a VBR-RT VC with a pending cell and with VC-credit greater than zero?
NO
YES
350
Schedule a cell corresponding to CBR VC
365
YES
Schedule a cell corresponding to the VBR-RT VC
Set VC-credit equal to zero
Decrement VC-credit of the VBR-RT VC by one
B
398
390
355
370
375
Schedule idle cell
NO
Any UBR VC with a pending cell?
NO
Is there a VBR-nRT VC with a pending cell and with VC-credit greater than zero
395
YES
YES
380
Schedule a cell corresponding to UBR VC
Schedule a cell corresponding to VBR-nRT VC
385
B
Decrement VC-credit of VBR-nRT VC by one

	401	402	403	404	405	406	407	408	
Line_Slot_Credit	100	200	100	200	100	200	100	200	441
Cell Slot	0	VCl	0	VC1	0	VC1	0	VC1	442
Line_Slot_balance	100	0	100	0	100	0	100	0	443
Cell Spacing	idle	VC1	idle	VC1	idle	VC1	idle	VC1	444
Transmitted Cell	idle	idle	idle	idle	idle	idle	idle	idle	445
VC-Credit	0	1	1	2	2	3	3	3	446

FIG. 4A

	451	452	453	454	455	456	457	458	459	460	
Line_Slot_Credit	100	200	175	150	125	100	200	175	150	125	461
Cell Slot	0	CBR	CBR	CBR	CBR	0	CBR	CBR	CBR	CBR	462
Line_Slot_balance	100	75	50	25	0	100	75	50	25	0	463
Line_Slot_Credit	100	200	100	200	100	200	100	200	100	200	464
Cell Slot	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	465
Line_Slot_balance	100	0	100	0	100	0	100	0	100	0	466
Cell Spacing	idle	CBR / VBR -nRT	CBR	CBR / VBR -nRT	CBR	VBR -nRT	CBR	CBR / VBR -nRT	CBR	CBR / VBR -nRT	467
Transmitted Cell	idle	CBR	CBR	CBR	VBR -nRT	VBR -nRT	VBR -nRT	VBR -nRT	idle	VBR -nRT	468
VC-Credit (CBR)	0	0	0	0	1	1	1	1	1	1	469-A
VC-Credit (VBR-nRT)	0	0+1 - 0= 1	1+0- 0= 1	1+1- 0=2	2+0- 1=1	1+1- 1=1	1+0- 1=0	0+1- 1=0	0+0- 0=0	0+1- 1=0	469-B

FIG. 4B

	471	472	473	474	475	476	477	478	479	480	
Line_Slot_Credit	100	200	175	150	125	100	200	175	150	125	481
Cell Slot	0	CBR	CBR	CBR	CBR	0	CBR	CBR	CBR	CBR	482
Line_Slot_balance	100	75	50	25	0	100	75	50	25	0	483
Line_Slot_Credit	100	200	100	200	100	200	100	200	100	200	484
Cell Slot	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	485
Line_Slot_balance	100	0	100	0	100	0	100	0	100	0	486
Cell Spacing	idle	CBR / VBR -nRT	CBR	CBR / VBR -nRT	CBR	VBR -nRT	CBR	CBR / VBR -nRT	CBR	CBR / VBR -nRT	487
Peak_Slot_credit	100	200	200	200	200	158	116	200	158	116	488
Transmitted Cell	idle	CBR	CBR	CBR	VBR -nRT	VBR -nRT	Idle	VBR -nrt	VBR -nRT	Idle	489
Peak_Slot_balance	100	200	200	200	58	16	116	58	16	116	490
VC-Credit (VBR-nRT)	0	0+1 - 0= 1	1+0- 0= 1	1+1- 0=2	2+0- 1=1	1+1- 1=1	1+0- 0=1	1+1- 1=1	1+0- 1=0	0+1- 0=1	491

FIG. 4C

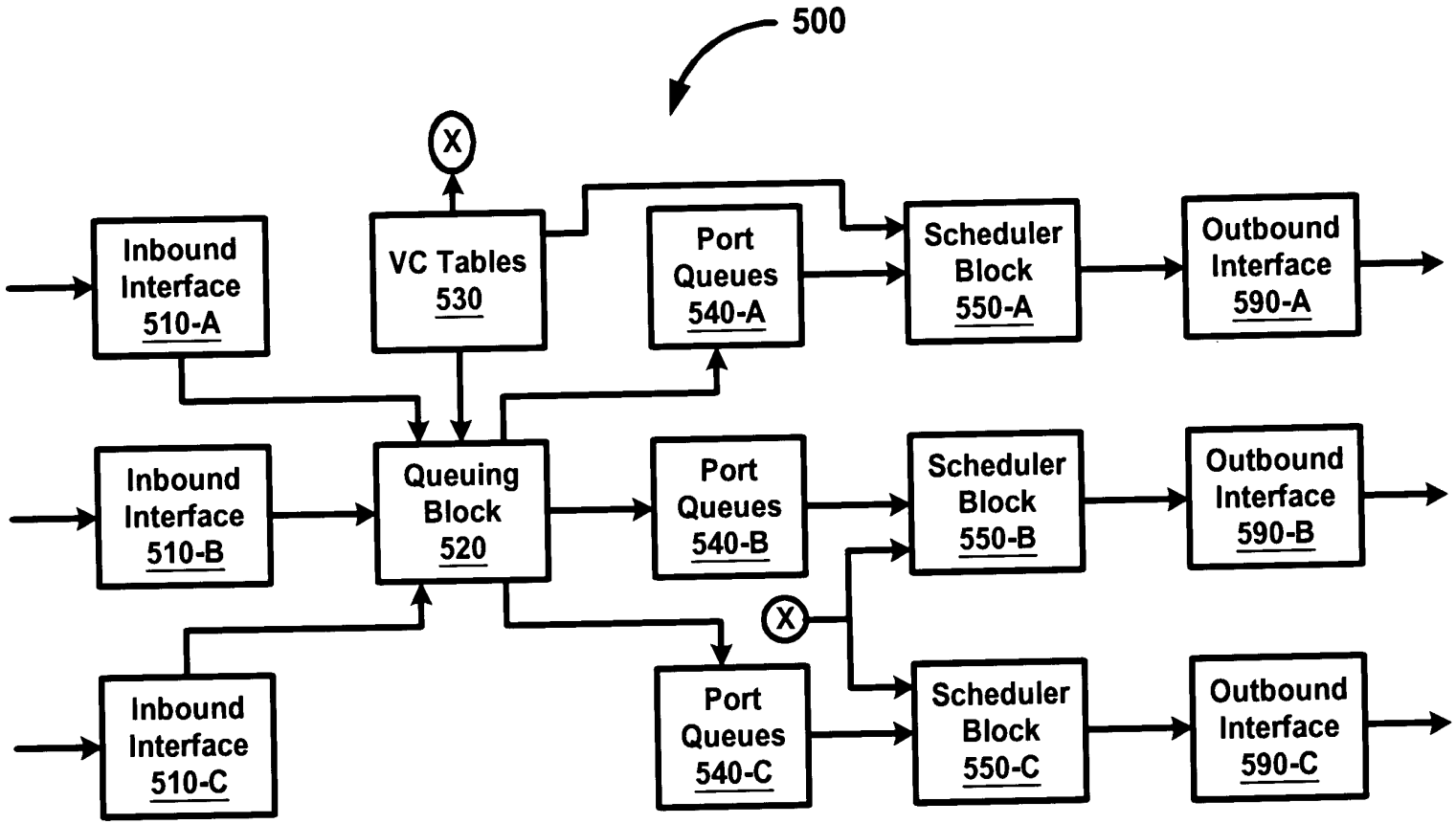

500
X
Inbound Interface 510-A
VC Tables 530
Port Queues 540-A
Scheduler Block 550-A
Outbound Interface 590-A
Inbound Interface 510-B
Queuing Block 520
Port Queues 540-B
Scheduler Block 550-B
Outbound Interface 590-B
X
Inbound Interface 510-C
Port Queues 540-C
Scheduler Block 550-C
Outbound Interface 590-C

FIG. 5

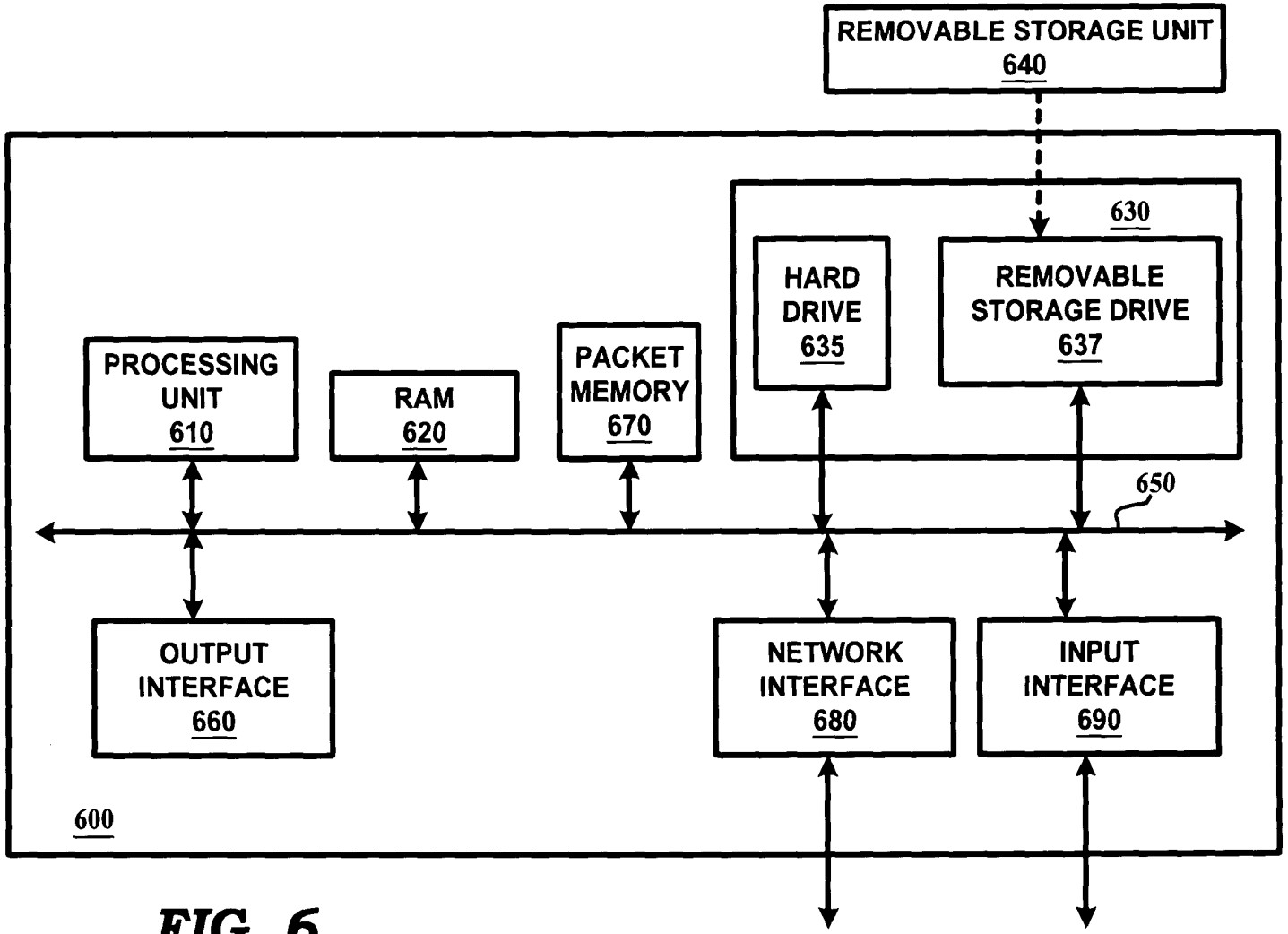

REMOVABLE STORAGE UNIT
640
630
HARD
DRIVE
635
REMOVABLE
STORAGE DRIVE
637
PROCESSING
UNIT
610
RAM
620
PACKET
MEMORY
670
650
OUTPUT
INTERFACE
660
NETWORK
INTERFACE
680
INPUT
INTERFACE
690
600

FIG. 6